10a and 10b and the description thereof. No new matter is added. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

Applicant believes that payment for one additional independent claim is needed. Accordingly, Applicant attaches hereto a check in the amount of $84.00 for one additional independent claim. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 23-1951.

Allowed Claims

Applicant appreciates the indication that claims 1-12 are allowed. Applicant further appreciates the indication that claims 34, 37-45 and 49 contain allowable subject matter. By this amendment, allowable claims 34, 37 and 38 are amended to independent format to include the features of base claim 29 and all respective intervening claims. Claim 46 is also amended to include the word "photodefinable" which distinguishes this claim over the applied references.

Applicant now submits that claims 34, 37, 38 and 46 and all respective dependent claims therefrom are in immediate condition for allowance. Applicant further submits that independent claim 29, as amended, and all dependent claims therefrom are also in condition for allowance. Therefore, Applicant submits that the entire application is now in condition for allowance and should pass to issuance.

§§102(b) and 103(a) Rejections

Claims 29 and 31 were rejected under 35 U.S.C. §102(b) over U.S. Patent No. 6,104,462 to Kurosaki. Claim 30 was rejected under §103(a) over Kurosaki in view of U.S. Patent No. 6,124,917 to Fujioka. Claims 32 and 33 were rejected under §103(a) over Kurosaki in view of U.S. Patent No. 6,300,152 to Kim. Claims 35, 36 and 46-48 were rejected under §103(a) over Kurosaki in view of U.S. Patent No.6,130,443 to Hong et al. These rejections are respectfully traversed.

Discussion of Invention

The present invention is directed to a thin film transistor array panels and the

manufacturing methods of the same. In LCD systems, a liquid crystal display (LCD) has two panels having electrodes for generating electric fields and a liquid crystal layer interposed therebetween. The transmittance of incident light is controlled by the intensity of the electric field applied to the liquid crystal layer. In the most widely used liquid crystal display, the field-generating electrodes are provided at both of the panels, with one of the panels having switching elements such as thin film transistors, and the other panel having color filters. In prior art LCD manufacturing processes, a thin film transistor array panel is manufactured by a photolithography process using five or six photomasks and a color filter panel manufactured by a photolithography process using three or four photomasks. Since the photolithography processes are expensive, the number of the photolithography steps needs to be minimized.

The present invention provides methods for manufacturing thin film transistor array panels for liquid crystal displays with a reduced number of masks employed in the photolithography processes. This is accomplished by forming a portion of a photoresist layer (photoresist) that is thinner than another portion between a source electrode and a drain electrode before the two electrodes are formed. Thus, the thin portion protects underlayers when some layers are etched, and is also etched along with other layers to expose its underlayer. Also, red, green, and blue color filters may be used as a passivation layer covering a thin film transistor and wires. A wire may be formed of a photosensitive conductive material.

In the manufacturing method according to the present invention, a gate wire including a gate line and a gate electrode connected to the gate line is formed on an insulating substrate. A gate insulating layer pattern covering the gate wire, a semiconductor pattern, and an ohmic contact layer pattern are formed. A data wire including a data line, a source electrode and a drain electrode is formed. The source electrode and the drain electrode are made of the same layer on the ohmic contact layer and separated from each other. The data line is connected to the source electrode. Then, red, green, and blue color filters covering the data wire is formed. The color filter has a first contact hole exposing the drain electrode. A pixel electrode is formed and connected to the drain electrode through the first contact hole. Here, the source electrode and the drain electrode are separated by a photolithography process using a photoresist pattern, and the photoresist pattern has a first portion having a first thickness that is at least located between the

source electrode and the drain electrode, a second portion having a second thickness thicker than the first portion, and a third portion having a third thickness thinner than the first thickness.

§102(b) Rejection
of Claims 29 and 31

Applicant first submits hat the Kurosaki reference was issued on August 15, 2000. The filing date of the present invention is April 26, 2000. However, the Kurosaki issue date is not more than one year from the filing date of the present invention. Accordingly, the §102(b) rejection is improper.

Second, assuming the Examiner is rejecting the claims under another provision of §102 (i.e., §102(e)). Applicant submits that in rejecting a claimed invention under §102, a single prior art reference must contain each and every limitation of the claim, either expressly or under the doctrine of inherency. *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1570 (Fed. Circ), cert denied, 488 U.S. 892 (1988). To "contain" the limitation the reference must explicitly describe the limitation, or describe an operation inherently requiring the limitation, completely enough to place limitation "in the possession of the public." *In re Epstein*, 32 F.3d 1559, 31 USPQd 1817 (Fed. Cir. 1994).

In the present rejection, Applicant submits that the Kurosaki does not show all of the features of the claimed invention. Specifically, the claimed invention recites, in part,

> forming a portion of a photoresist layer that is thinner than another portion between a source electrode and a drain electrode before forming the source electrode and the drain electrode such that the thin portion protects at least a portion of data wire during an etching process while also being etched to expose ohmic contact layer.

However, this same feature is not shown in the Kurosaki reference. In Kurosaki, fabrication steps are shown in Figures 2, 3 and 7 and also described at col. 7. In these steps, a metal is formed on a glass substrate 4 by a sputtering method. A pattern is then formed in a predetermined shape by photolithography method. Thus, a scanning line and a gate electrode 11

are formed. A gate insulation film 12 is formed on the pattern and, thereafter, a semiconductor layer 19 and a channel protection film 14 are formed. Next, a signal line, a drain electrode 16, and a source electrode 18 are formed. Nega-resists containing pigments of red (R), green (G), and blue (B) are also patterned by a photolithography method. Thus, a color filter layer 7 having R, G, and B color filters is formed at the same time a pedestal 13 is formed. Thereafter, black nega-resists containing pigments of R, G, and B are patterned. In this manner, a column shaped spacer 25 and an organic film 2 are formed. At that point, the organic film 2 is formed so that it covered to the center of the pedestal 13. Next, a conductor layer is formed and, after a resist is coated, a pixel electrode 8 is patterned by an etching method. The source electrode 18 is connected to the pixel electrode 8 above the color filter layer 7 through a contact hole of the color filter layer 7. As seen, there is no disclosure, whatsoever, of the features of the claimed invention.

Applicant now submits that the §102(b) rejection should be withdrawn and that claim 29 and its dependent claims be allowed to pass to issue.

§103(a) Rejections

Claims 30, 32, 33, 35, 36 and 46-48 are all rejected under §103(a) over Kurosaki in view of various references. Applicant submits that claims 32, 33, 35, 36, 47 and 48 are dependent claims and thus include all of the features of the respective distinguishable base claims. Specifically, claims 32, 33, 35 and 36 have their dependencies originating from distinguishable claim 29, and claims 47 and 48 depend from allowable claim 46. Accordingly, claims 30, 32, 33, 35, 36 and 46-48 are also distinguishable and are in condition for allowance.

In addition, the applied prior art references do not compensate for the deficiencies of Kurosaki and thus claims 30, 32, 33, 35, 36 and 46-48 should be in immediate condition for allowance.

Kim shows an organic insulating layer that is formed on an insulating substrate for an LCD having a gate electrode, a semiconductor layer, and a source and drain electrode, and that is patterned to form a contact hole exposing the drain electrode. The organic insulating layer is treated with argon plasma to remove residues of the organic insulating layer and to increase its

surface roughness. Next, a transparent insulating layer, such as an ITO layer, is deposited and patterned to form a pixel electrode connected to the drain electrode through the contact hole.

Fujioka shows a liquid crystal display device which includes a pair of opposite substrates, and a liquid crystal layer as a display medium disposed between the substrates. The pair of substrates are adhered together by a resin sealing material disposed on the periphery portion of at least one of the substrates at the prescribed gap, and an outflow preventing portion having a plurality of concave portions is provided so that at least a part of the outflow preventing portion overlaps with the sealing material.

Hong shows a liquid crystal display which has wires made of aluminum alloy layer, and two molybdenum-tungsten alloy layers located on under the aluminum alloy layer, respectively. To form a wire, the first molybdenum-tungsten alloy layer, the aluminum alloy layer, and the second molybdenum-tungsten alloy layer are sequentially deposited. The first molybdenum-tungsten alloy layer has a lower etch rate than that of the aluminum layer or the aluminum alloy layer, and the second molybdenum-tungsten alloy layer has a higher etch rate than that of the aluminum layer or the aluminum alloy layer.

On page 3 of the Office Action, the Examiner rejected claims 46-48 under 35 U.S.C. 103 as being unpatentable over Kurasaki et al. in view of Hong et al. Amended claim 46 includes the limitation "photodefinable" instead of "photosensitive". This photodefinable material is different than that of photosensitive which is commonly used for a material changing its chemical structure when exposed to light.

Conclusion

Applicant appreciates the indication of allowable claims; however, submits that in view of the foregoing amendments and remarks, all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed.

Applicant makes a written conditional petition for extension of time, if required. Charge any deficiencies and credit any overpayment of fees to Attorney's Deposit Account No. 23-1951.

Respectfully submitted,

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Marked-Up Copy of Claims

The following is a marked-up copy of amended claims 29, 34, 37, 38 and 46.

29. (Amended) A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising steps of:

forming a gate wire including a gate line and a gate electrode connected to the gate line on an insulating substrate;

forming a gate insulating layer covering the gate wire;

forming a semiconductor pattern on the gate insulating layer;

forming a data wire including a source electrode [and], a drain electrode and a data line connected to the source electrode on [the ohmic contact layer] the semiconductor pattern so that a portion of the semiconductor pattern between the source electrode and the drain electrode are exposed;

forming [red, green, and blue] color filters[, said filters] made of photosensitive material, the filters [and] covering the data wire, directly contacting the exposed portion of the semiconductor pattern, and having a first contact hole, and

forming a pixel electrode connected to the drain electrode through the first contact hole of the color filters.

34. (Amended) [The method of claim 33,] A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising steps of:

forming a gate wire including a gate line and a gate electrode connected to the gate line on an insulating substrate;

forming a gate insulating layer covering the gate wire;

forming a semiconductor pattern on the gate insulating layer;

forming a data wire including a source electrode and a drain electrode and a data line connected to the source electrode on an ohmic contact layer;

forming red, green, and blue color filters, said filters made of photosensitive material and covering the data wire and having a first contact hole;

forming a pixel electrode connected to the drain electrode through the first contact hole of the color filters; and

forming a passivation layer covering a color filter before forming red, green, and blue color filters, the passivation layer being made of photosensitive transparent organic material having a good planarization property, wherein

the red, green, and blue color filters, and the passivation layer are patterned through only exposure and development to form the first contact hole,

the gate wire further includes a gate pad that is connected to and receives a signal from an external circuit, and the data wire further includes a data pad that is connected to and receives a signal from an external circuit, and the color filter, the passivation layer, and the gate insulating layer have a second contact hole and a third contact hole respectively exposing the gate pad and the data pad, and

further comprising a step of forming a redundant gate pad and a redundant data pad that are made of the same layer as the pixel electrode and respectively connected to the gate pad and the data pad through the second contact hole and the third contact hole.

37. (Amended) [The method of claim 36,] A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising steps of:

forming a gate wire including a gate line and a gate electrode connected to the gate line on an insulating substrate;

forming a gate insulating layer covering the gate wire;

forming a semiconductor pattern on the gate insulating layer;

forming a data wire including a source electrode and a drain electrode and a data line connected to the source electrode on an ohmic contact layer;

forming red, green, and blue color filters, said filters made of photosensitive material and covering the data wire and having a first contact hole; and

forming a pixel electrode connected to the drain electrode through the first contact hole of the color filters, wherein

the gate wire or the data wire is made of photosensitive conductive material, and

the gate wire and the data wire are patterned through only exposure and development, and [the gate wire and the data wire] are made of Ag paste or copper organic metal that includes photoresist.

38. (Amended) [The method of claim 29,] A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising steps of:

forming a gate wire including a gate line and a gate electrode connected to the gate line on an insulating substrate;

forming a gate insulating layer covering the gate wire;

forming a semiconductor pattern on the gate insulating layer;

forming a data wire including a source electrode and a drain electrode and a data line connected to the source electrode on an ohmic contact layer;

forming red, green, and blue color filters, said filters made of photosensitive material and covering the data wire and having a first contact hole; and

forming a pixel electrode connected to the drain electrode through the first contact hole of the color filters,

wherein the source electrode and the drain electrode are separated by a photolithography process using a data wire pattern, and the data wire pattern has a first portion having a first thickness and is at least located between the source electrode and the drain electrode, a second portion having a second thickness thicker than the first portion, and a third portion having a third thickness thinner than the first thickness.

46. (Amended) A thin film transistor array panel for a liquid crystal display, comprising:

a gate wire including a gate line and a gate electrode connected to the gate line, and formed on an insulating substrate;

a gate insulating layer covering the gate electrode;

a semiconductor pattern formed on the gate insulating layer;

a data wire including a source electrode and a drain electrode, and a data line connected to the source electrode;

a passivation layer covering the data wire and having a first contact hole exposing the drain electrode; and

a pixel electrode connected to the drain electrode through the first contact hole,

wherein the gate wire or the data wire are made of [photosensitive] photodefinable conductive material.